Fig. 1A
SIDE VIEW

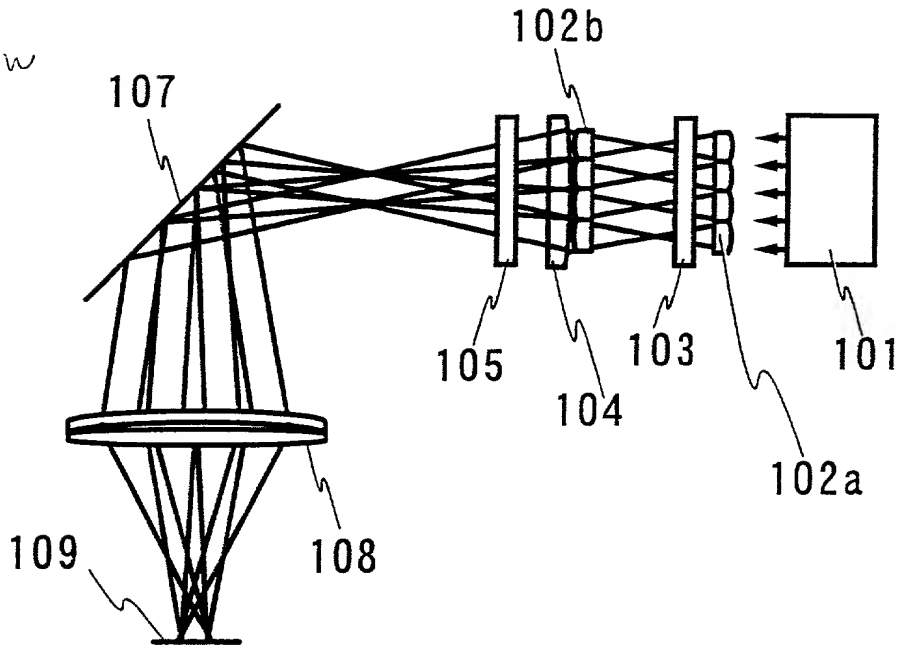
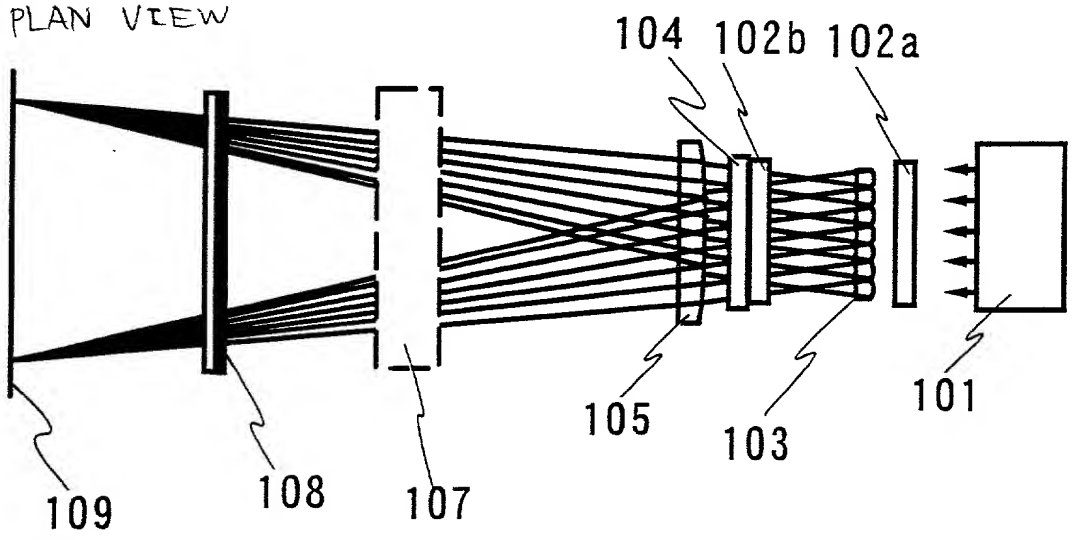


Fig. 1B
PLAN VIEW



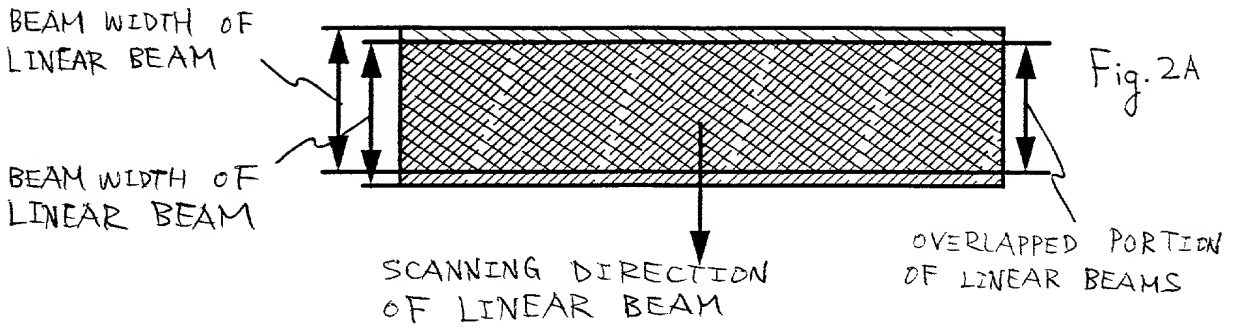


Fig. 2A

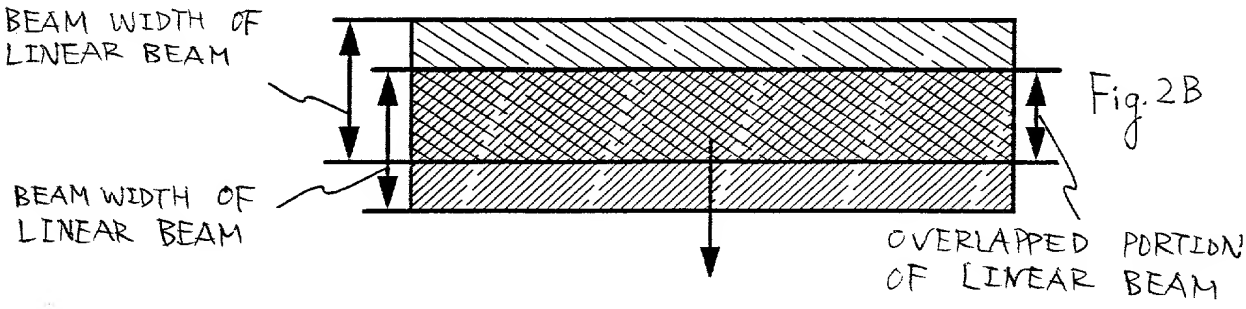


Fig. 2B

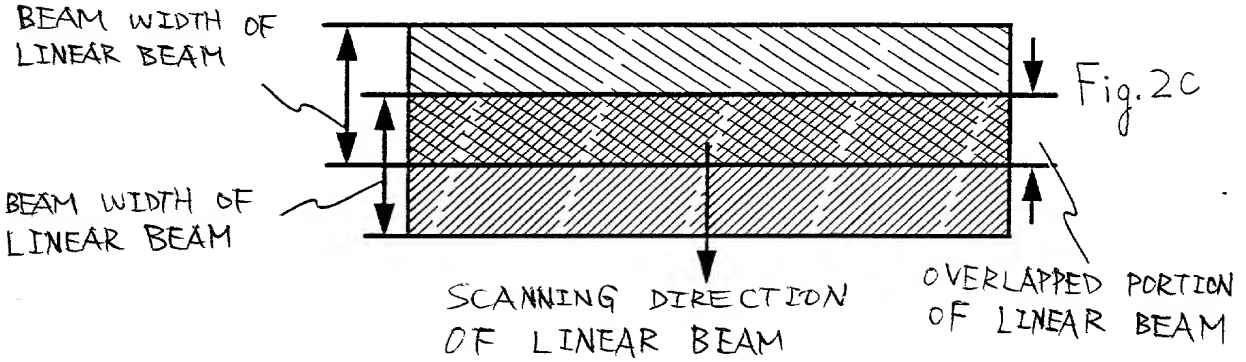


Fig. 2C

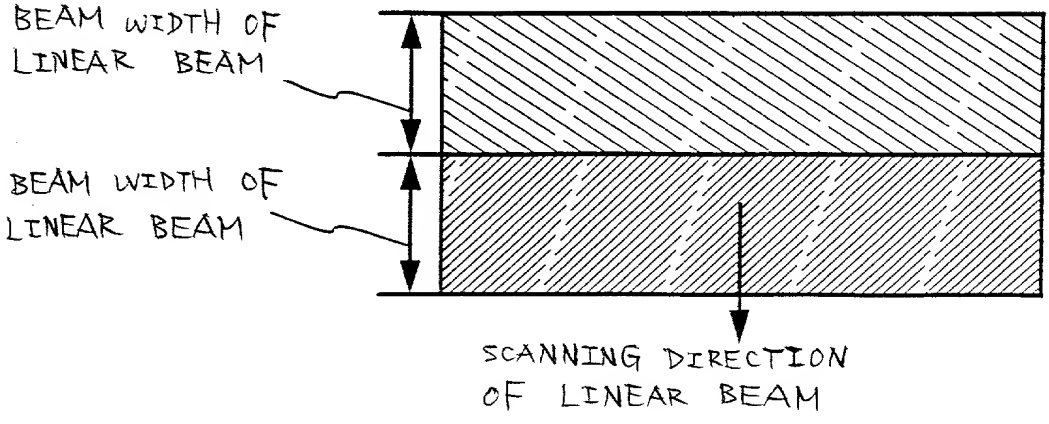


Fig. 2D

Fig. 3

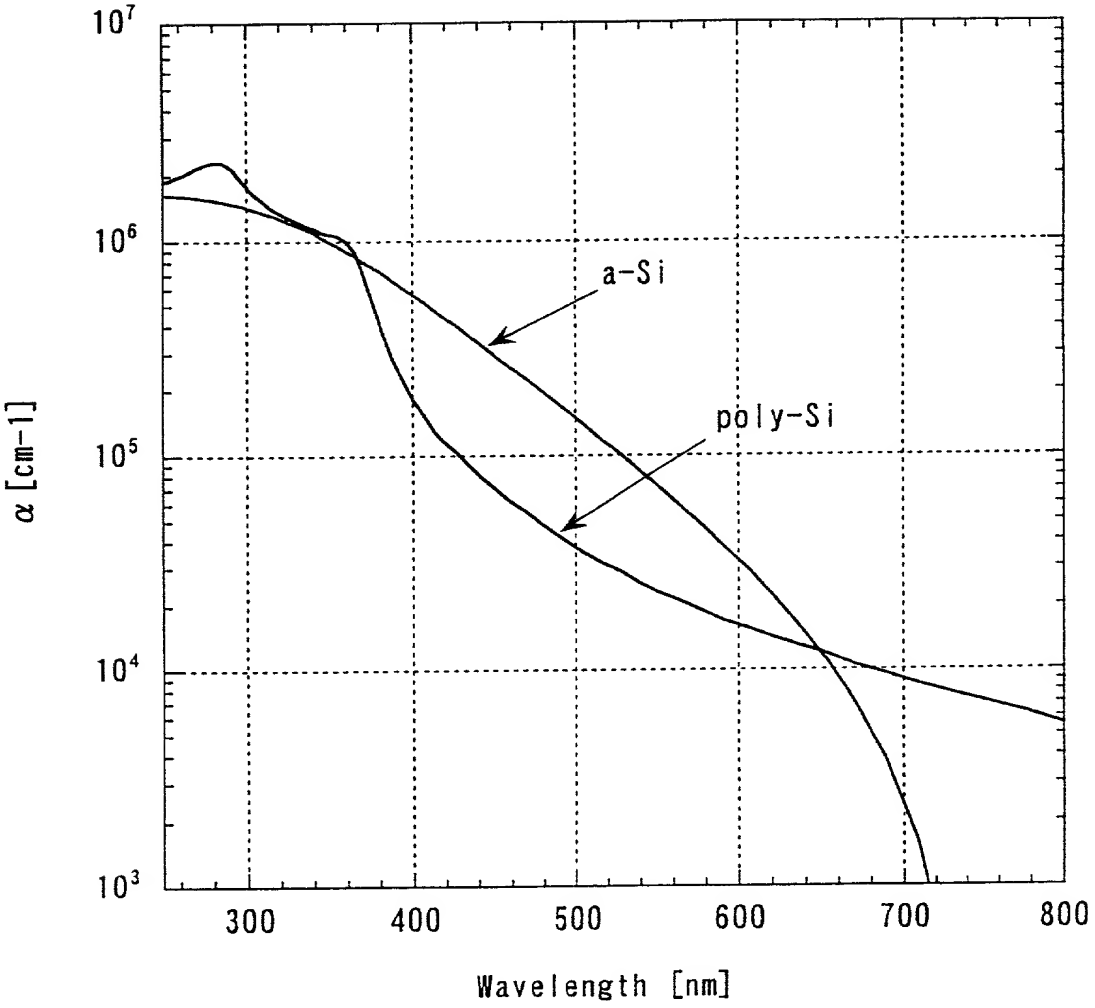

10^7
10^6
10^5
10^4
10^3
α [cm-1]
a-Si
poly-Si
300
400
500
600
700
800
Wavelength [nm]

Fig. 4A

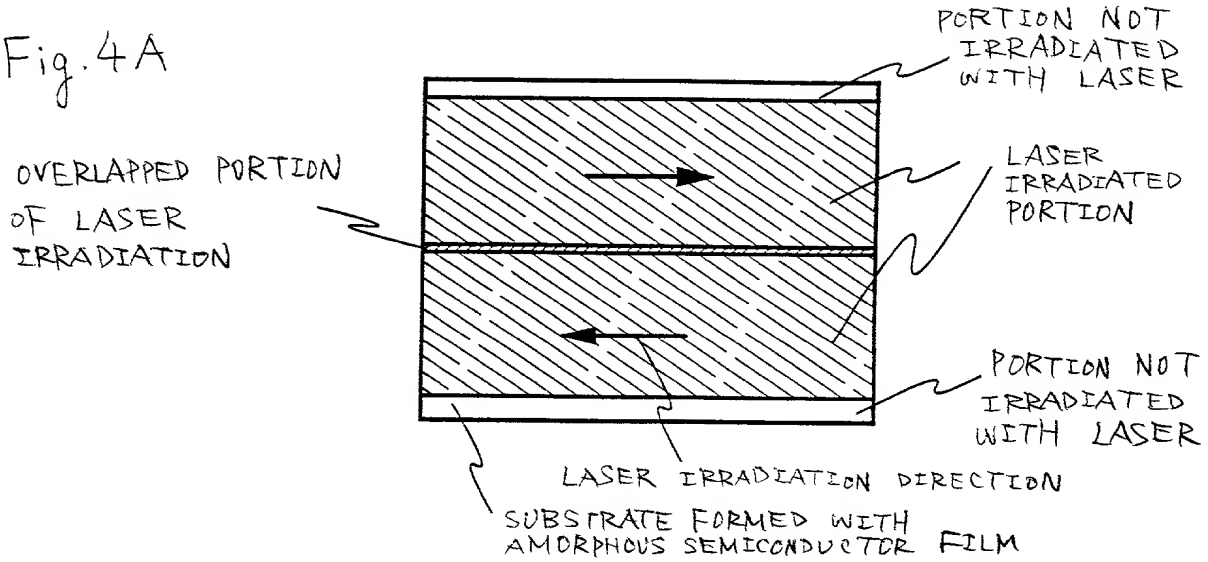


Fig. 4B

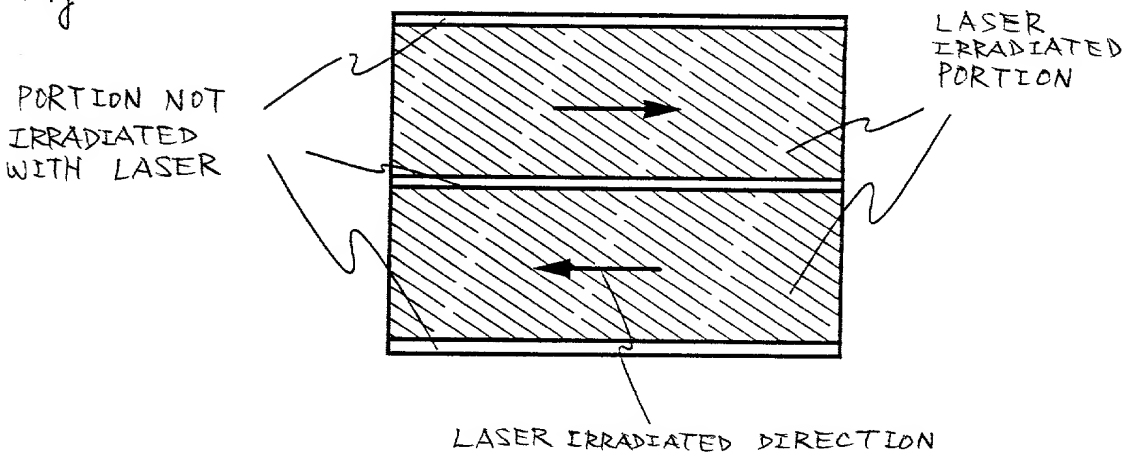


Fig. 4C

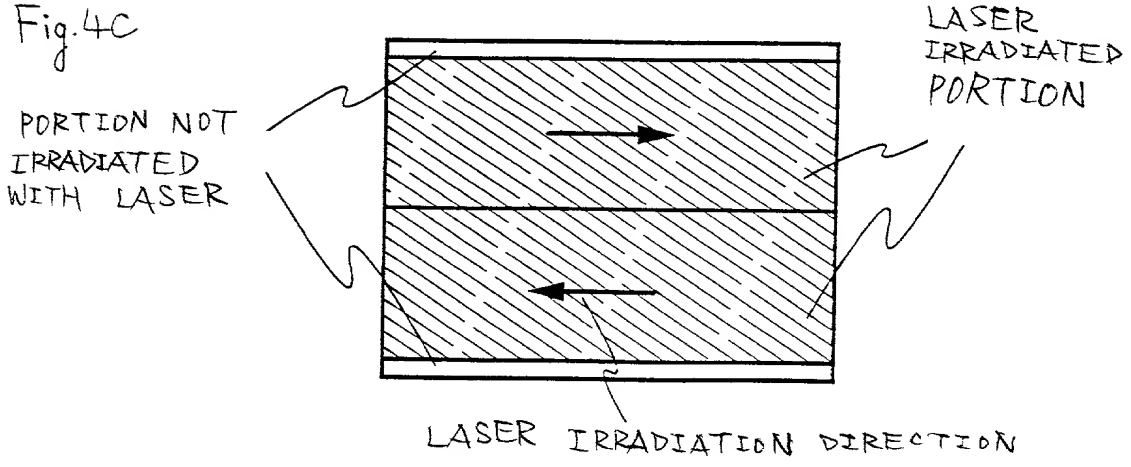


Fig.5A
SIDE VIEW

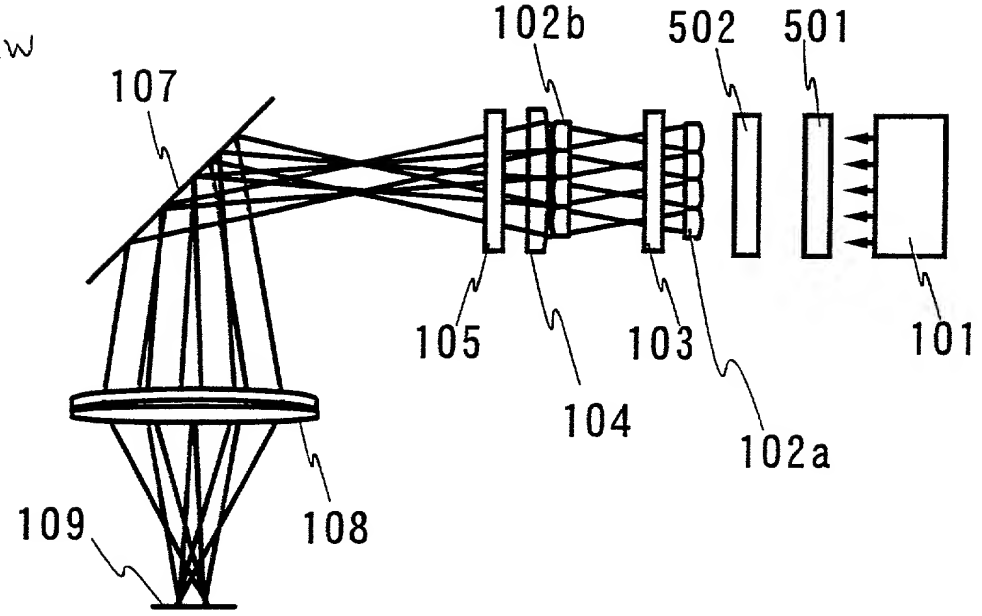
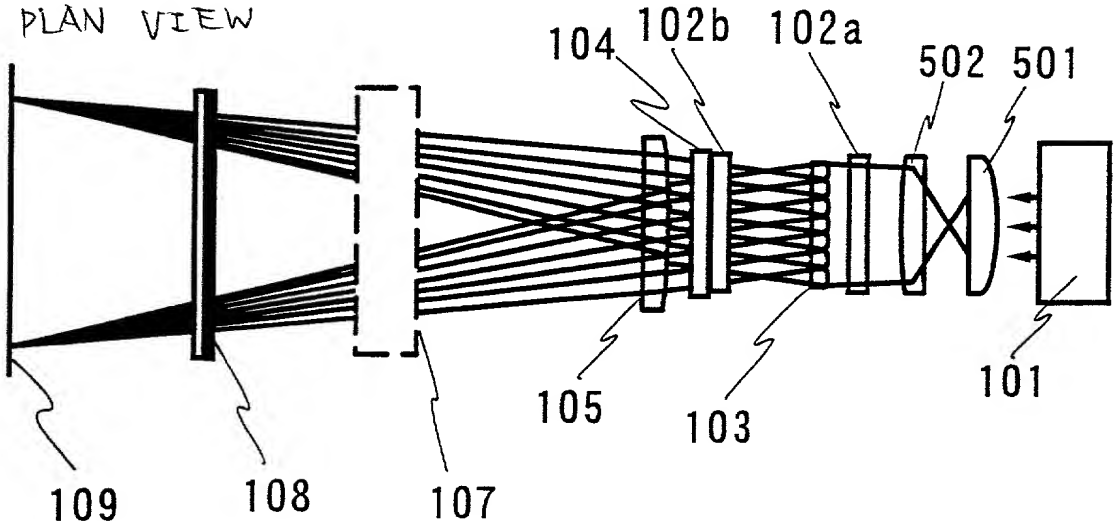


Fig.5B
PLAN VIEW



FORMATION OF UNDERLYING FILM AND AMORPHOUS SEMICONDUCTOR FILM

Fig.6A

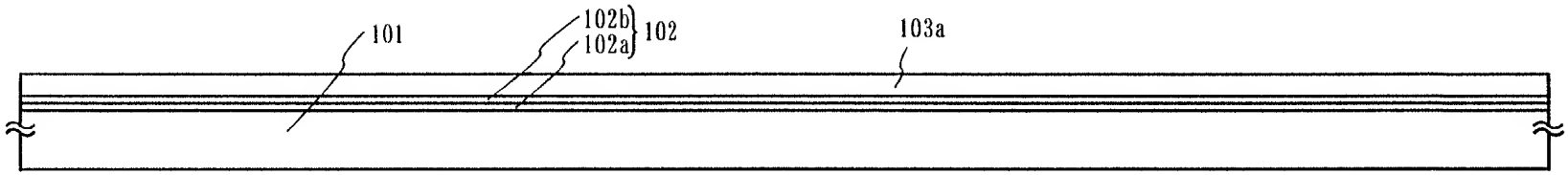


Fig.6B CRYSTALLIZATION PROCESS

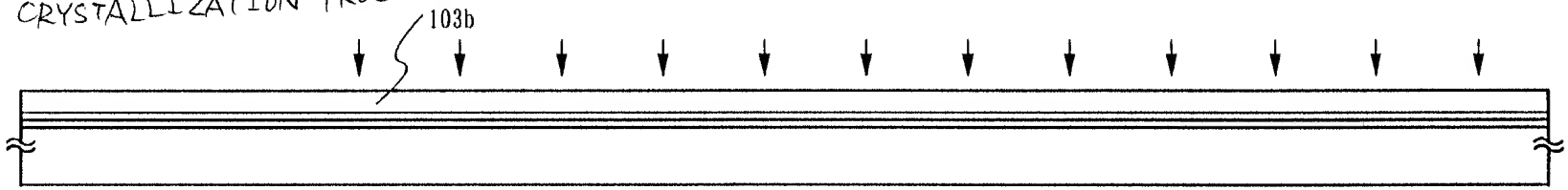


Fig.6C FORMATION OF ISLAND-SHAPED SEMICONDUCTOR LAYER AND GATE INSULATING FILM

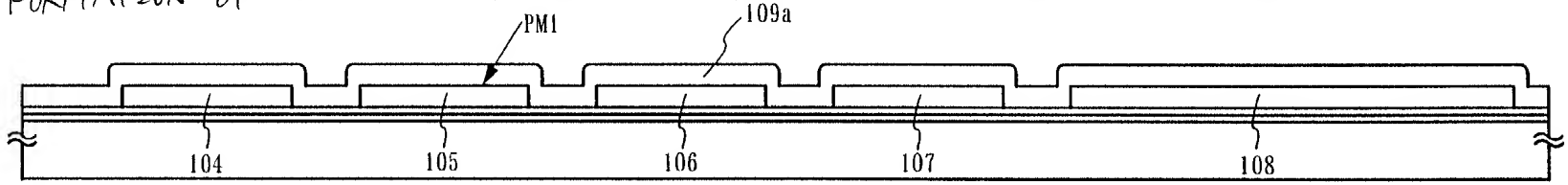


Fig.6D FORMATION OF HEAT-RESISTANT CONDUCTIVE LAYER

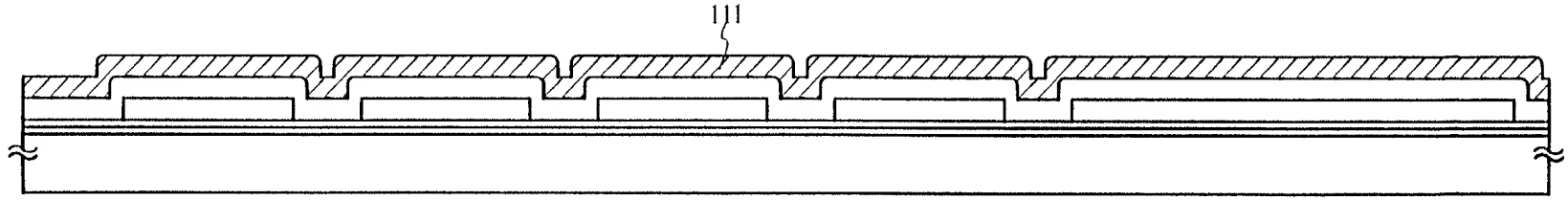


Fig.7A FIRST ETCHING PROCESS/ FIRST DOPING PROCESS (n^+)

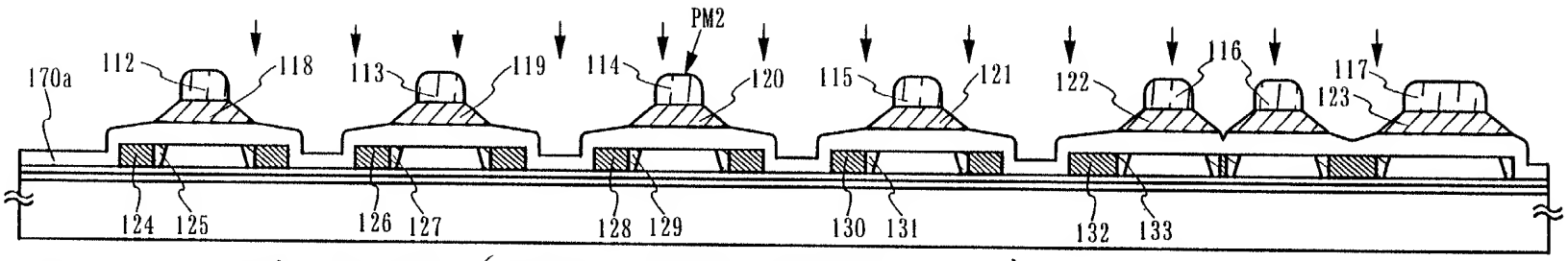


Fig.7B SECOND ETCHING PROCESS/ SECOND DOPING PROCESS (n^-)

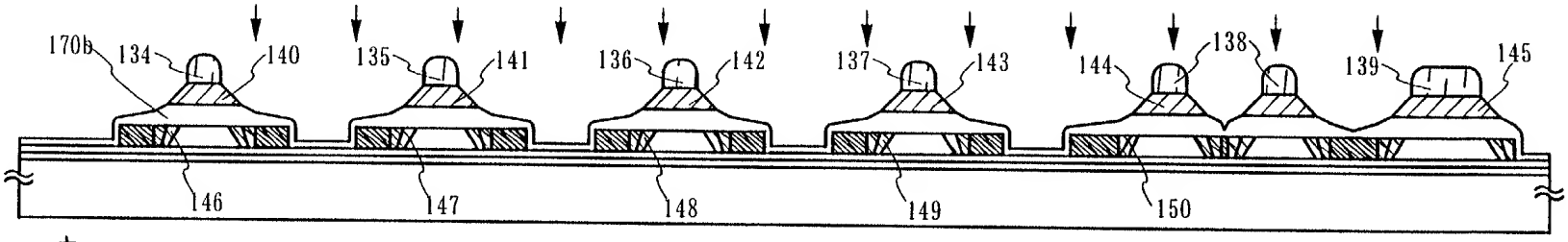


Fig.7C P^+ DOPING PROCESS

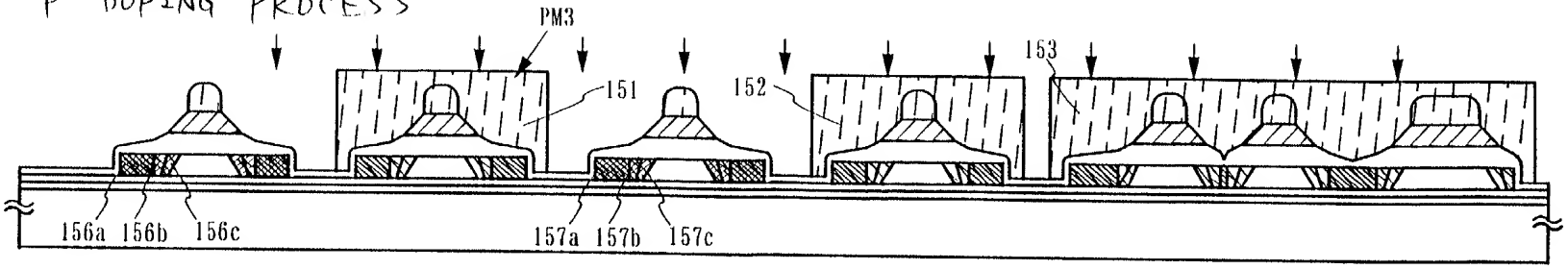


Fig. 8A FORMATION OF FIRST INTERLAYER INSULATING FILM

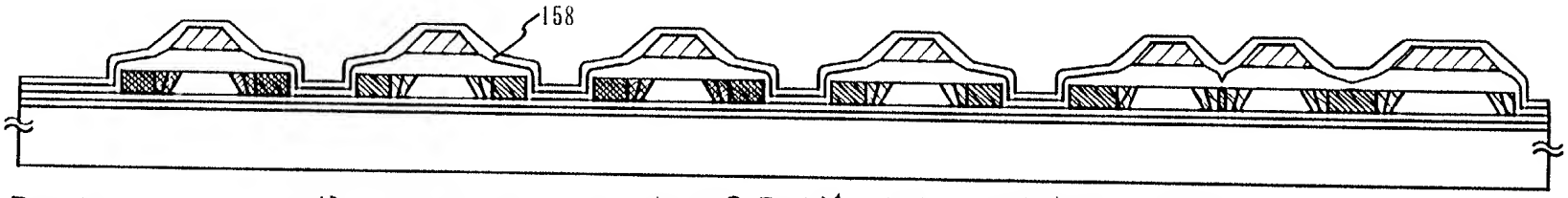


Fig. 8B FORMATION OF SECOND INTERLAYER INSULATING FILM AND CONTACT HOLE AND WIRING AND PIXEL ELECTRODE

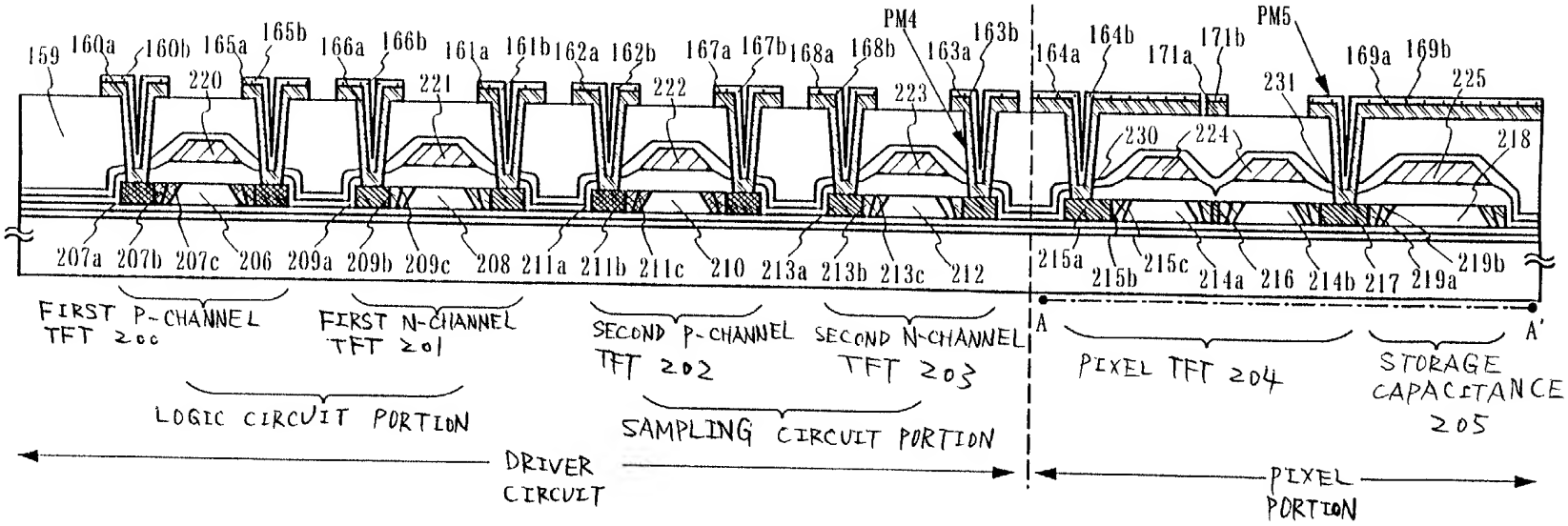


Fig. 9A

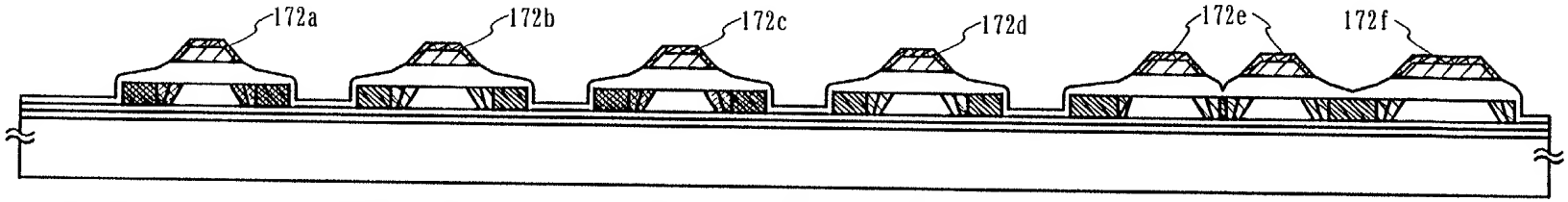


Fig. 9B FORMATION OF FIRST INTERLAYER INSULATING FILM

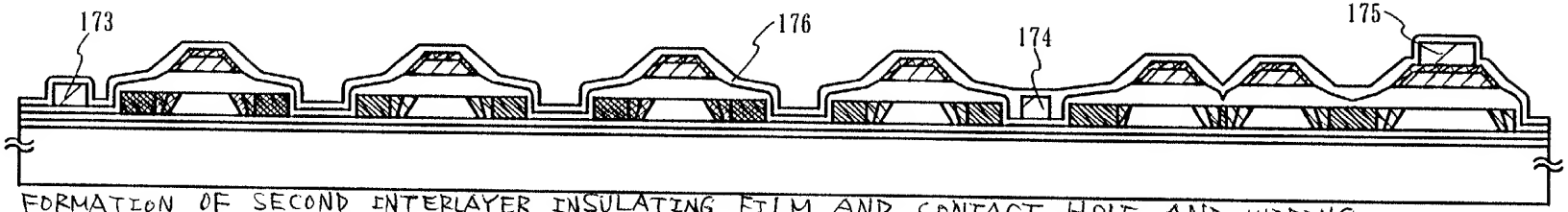
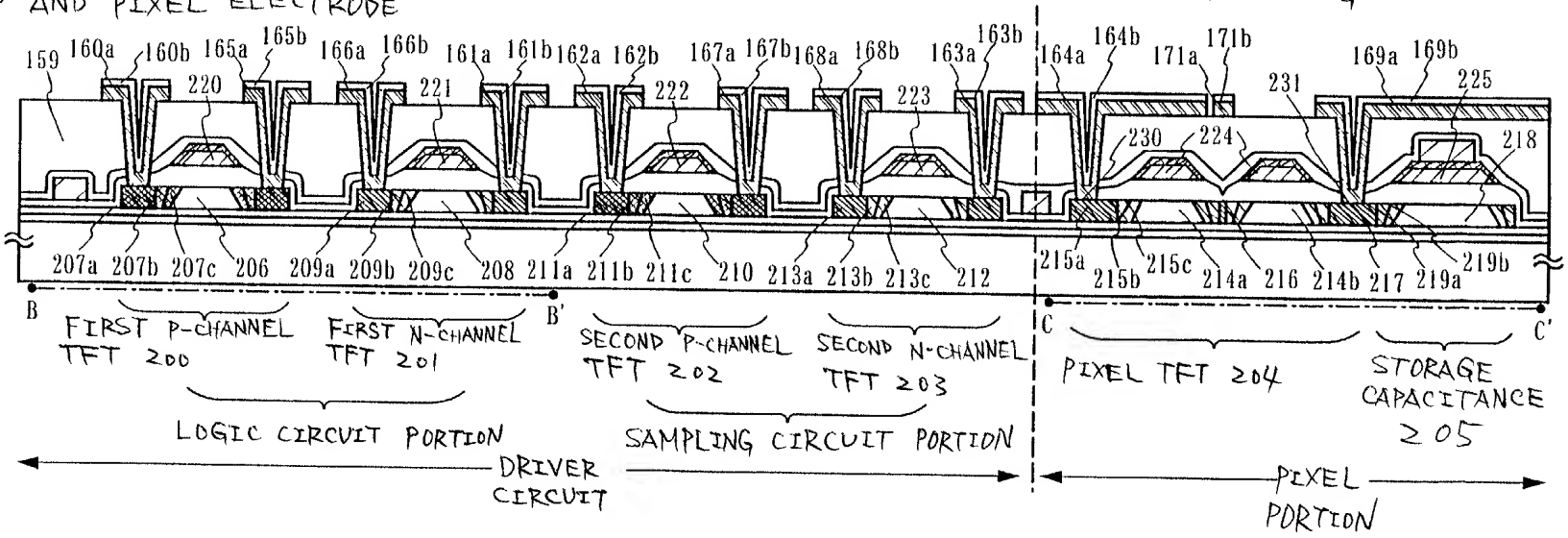


Fig. 9C FORMATION OF SECOND INTERLAYER INSULATING FILM AND CONTACT HOLE AND WIRING AND PIXEL ELECTRODE



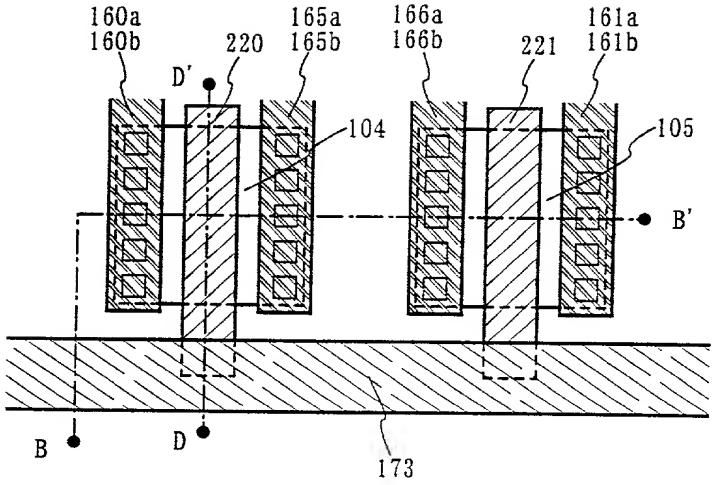


Fig. 10A

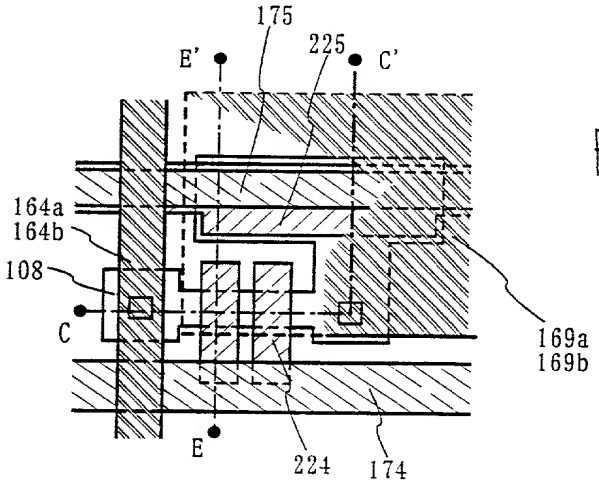


Fig. 10B

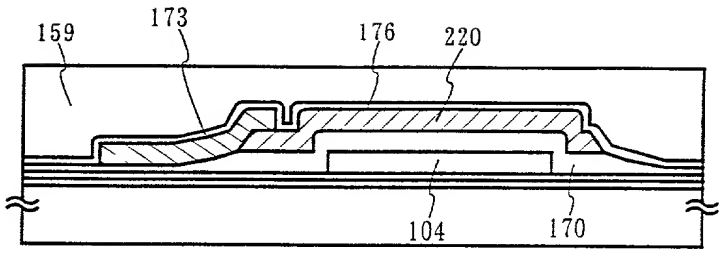


Fig. 11A

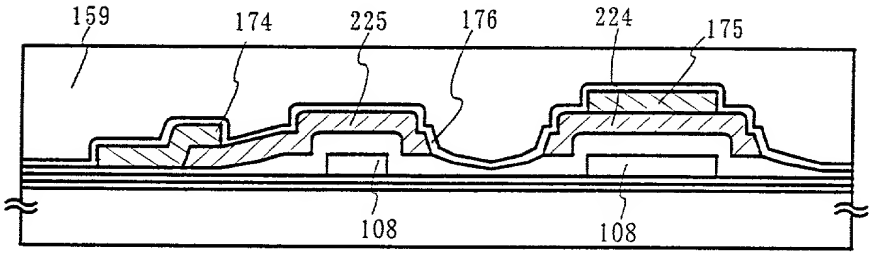


Fig. 11B

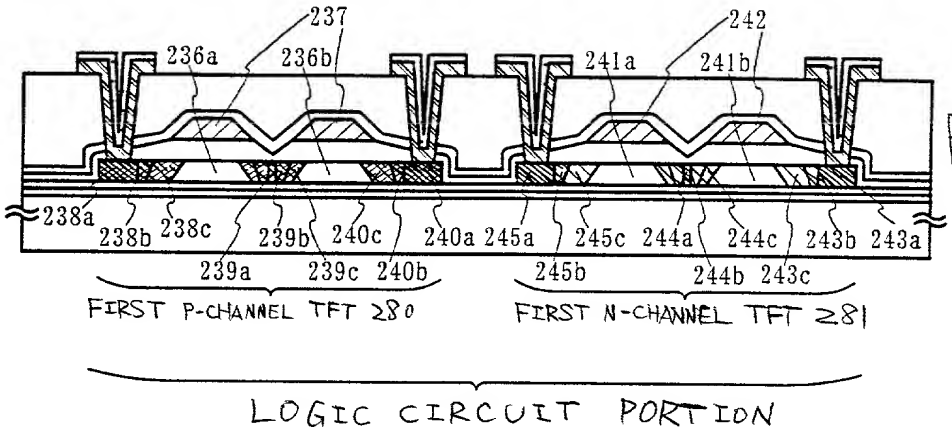


Fig. 12A

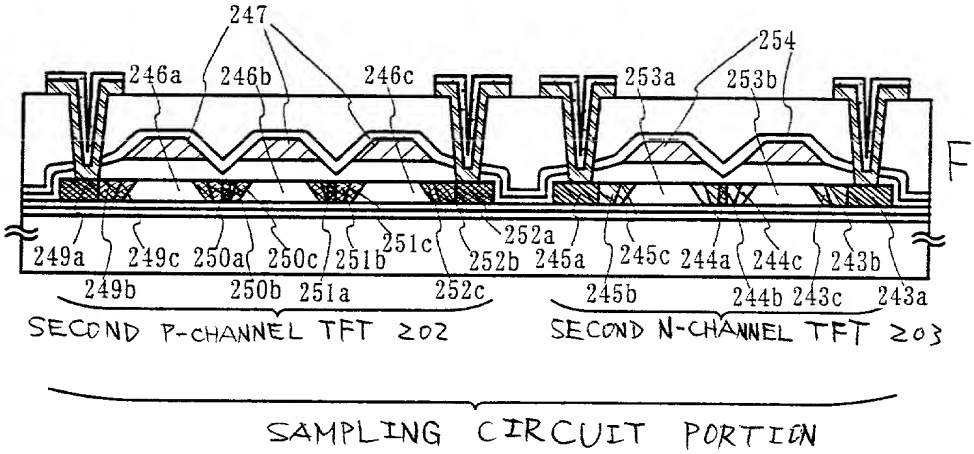


Fig. 12B

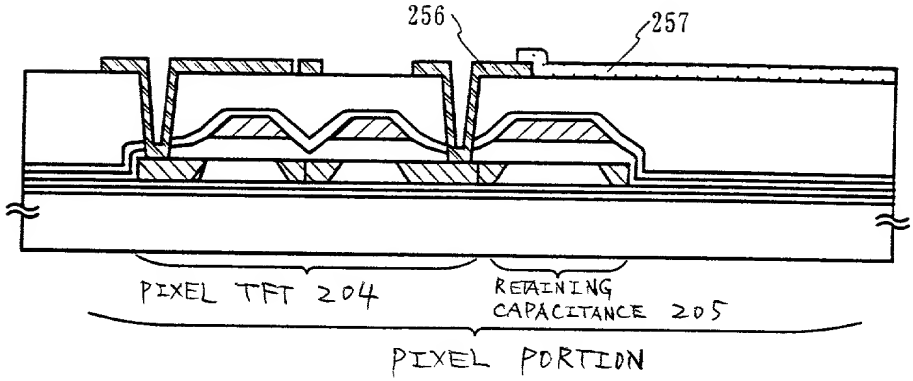


Fig. 13A

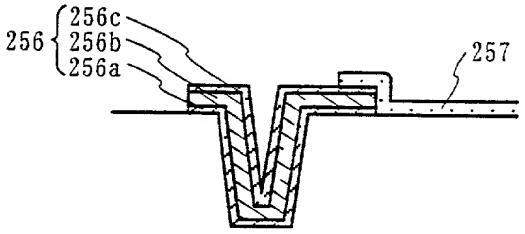


Fig. 13B

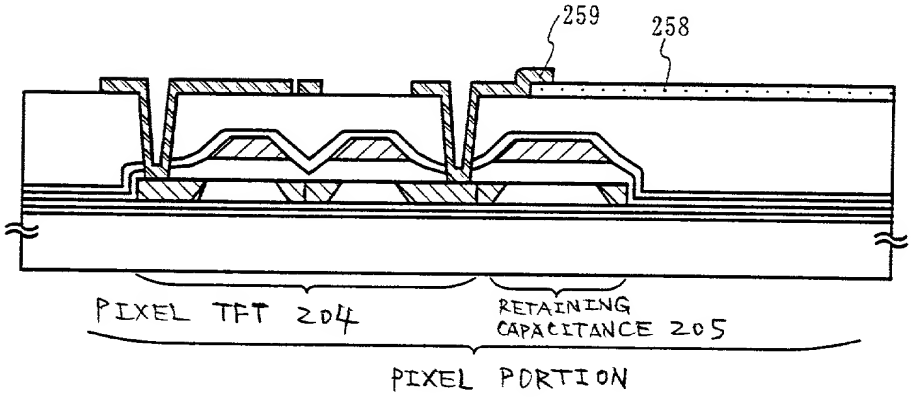


Fig. 13C

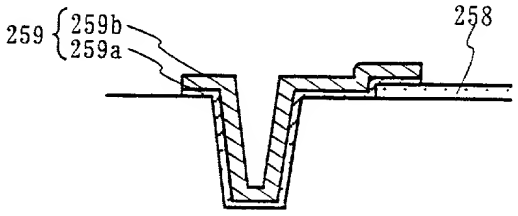


Fig. 13D

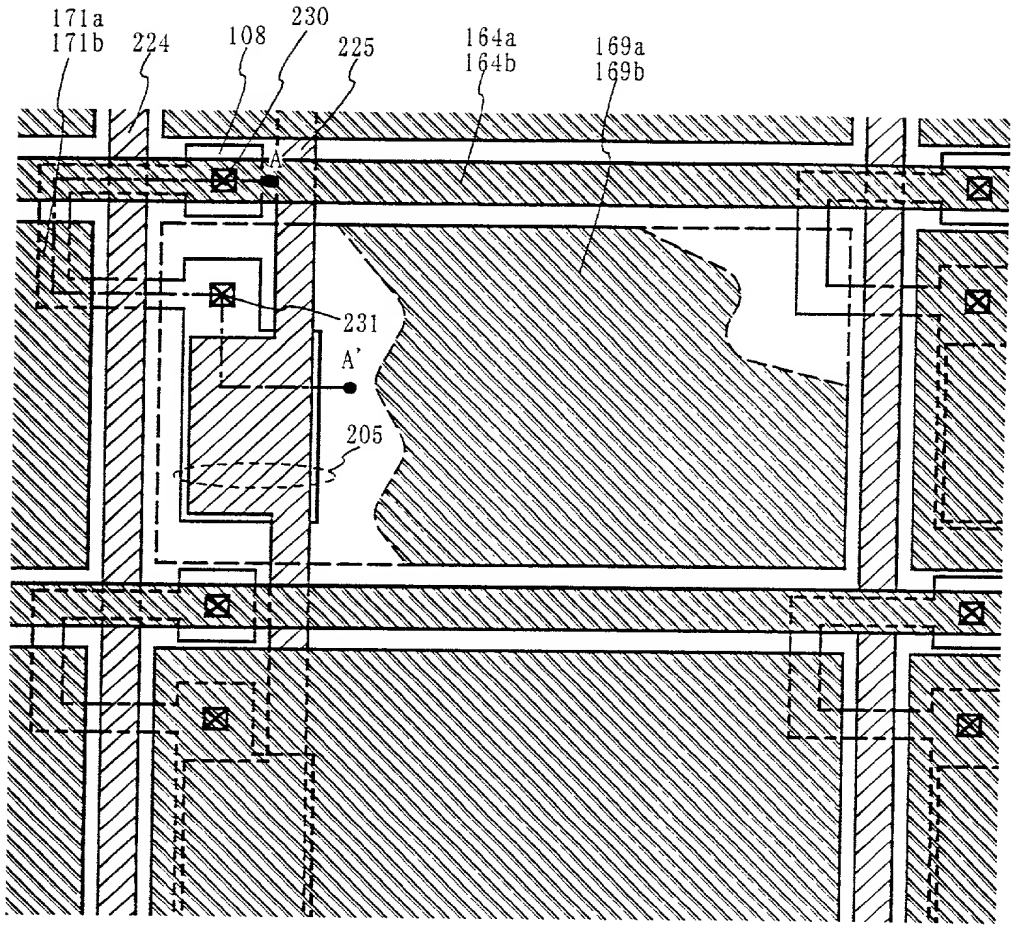


Fig.14

Fig.15A

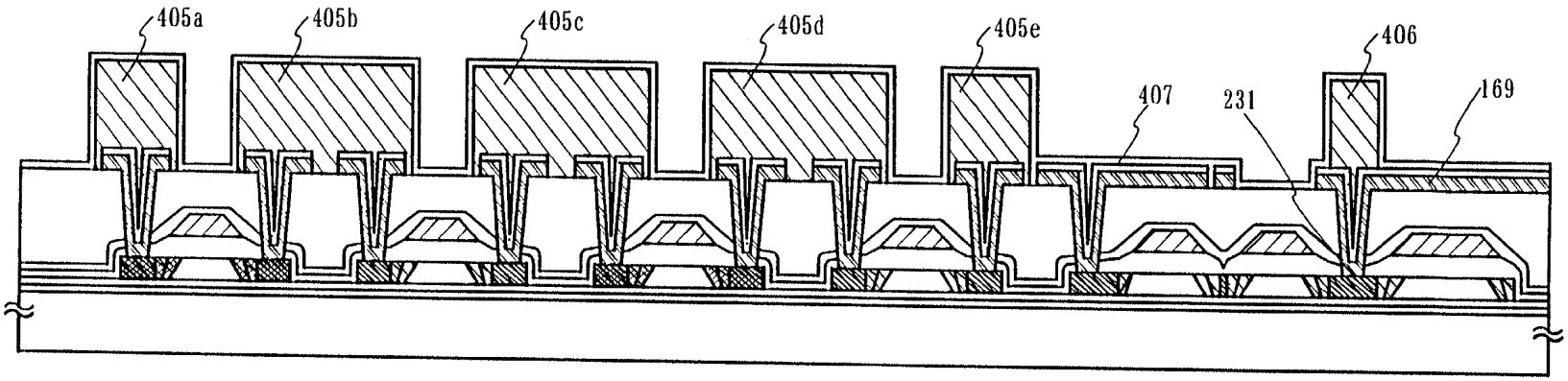
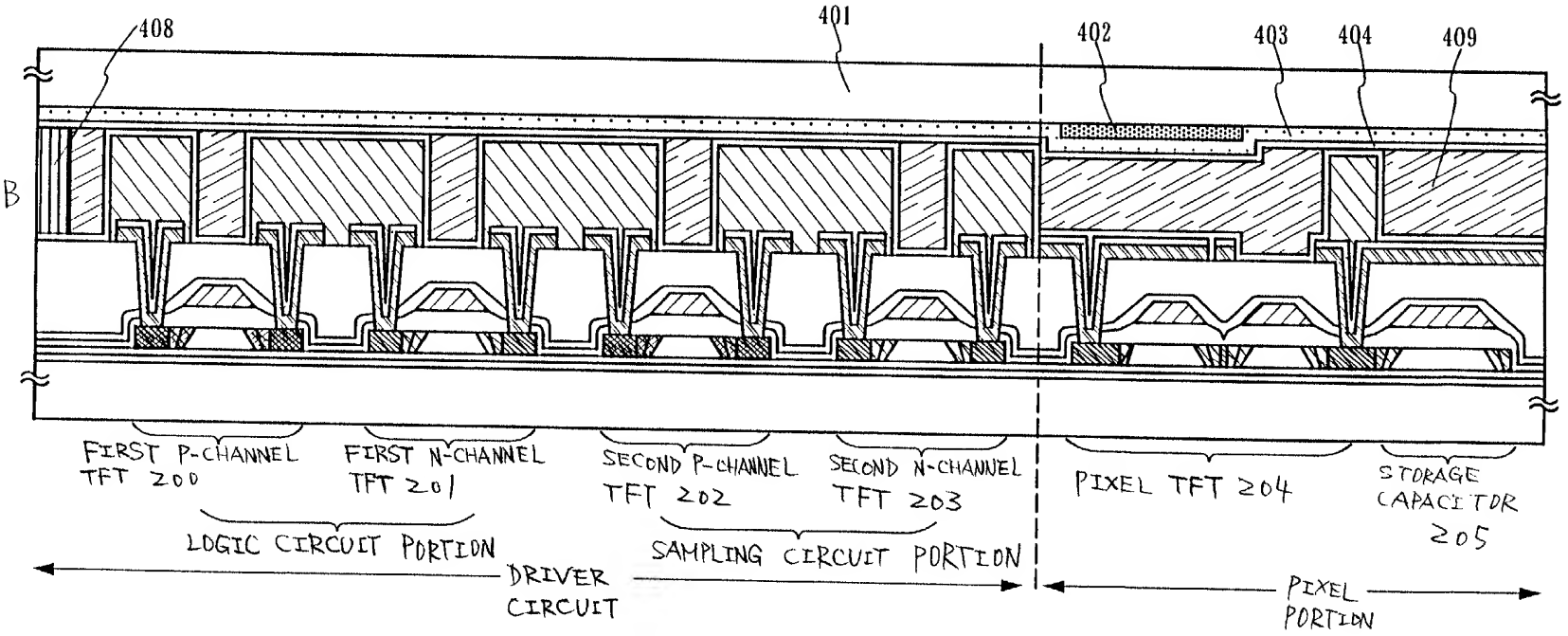


Fig.15B



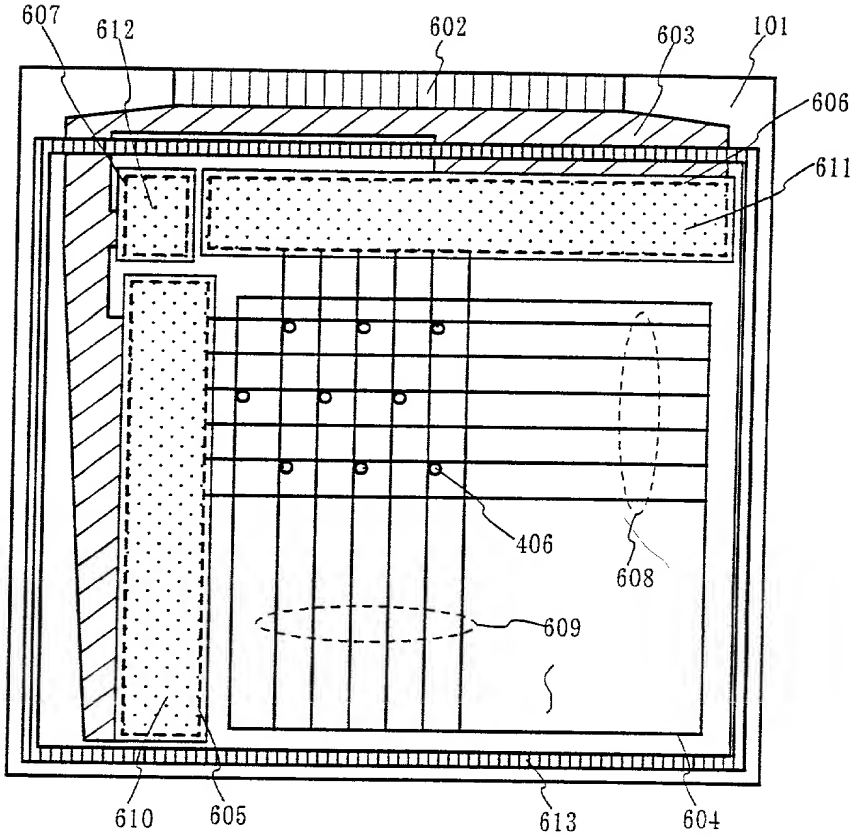


Fig. 16

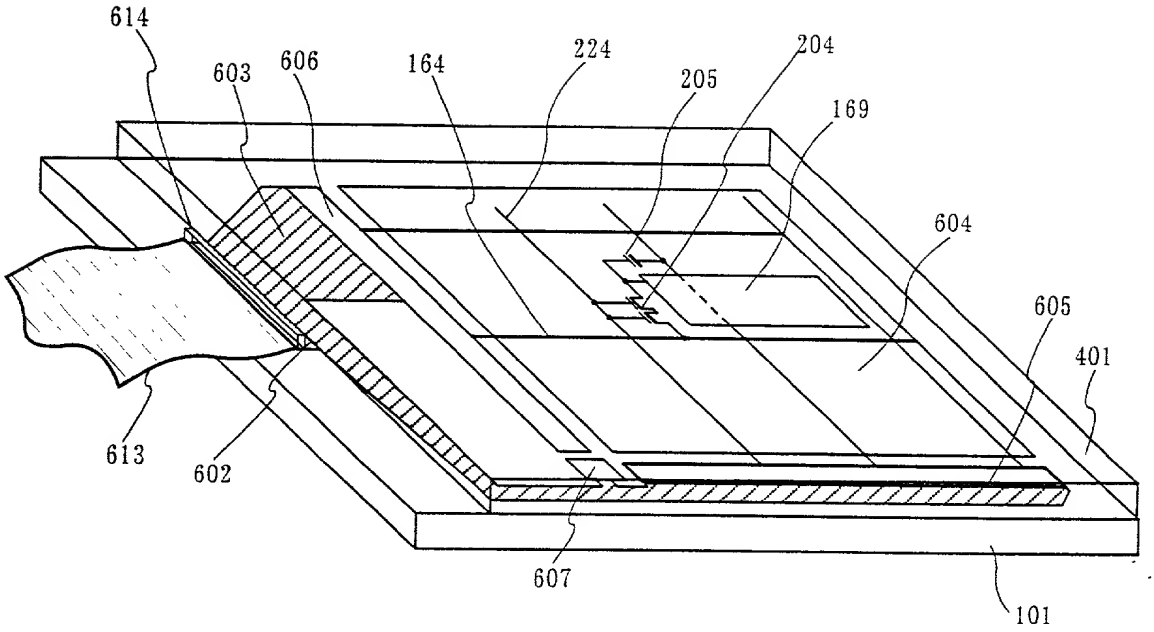


Fig. 17

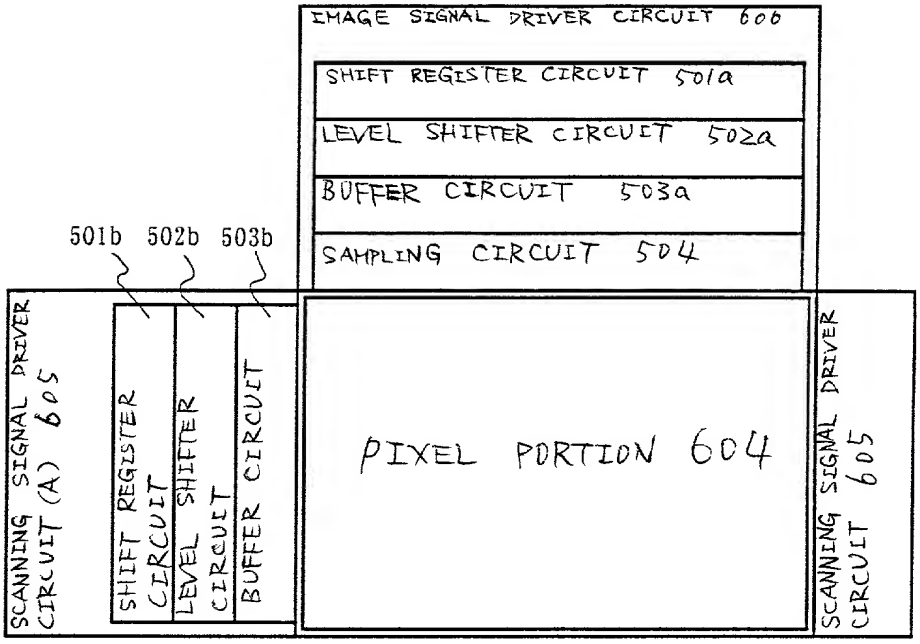


IMAGE SIGNAL DRIVER CIRCUIT 600
SHIFT REGISTER CIRCUIT 501a
LEVEL SHIFTER CIRCUIT 502a
BUFFER CIRCUIT 503a
SAMPLING CIRCUIT 504
501b
502b
503b
SCANNING SIGNAL DRIVER CIRCUIT (A) 605
SHIFT REGISTER CIRCUIT
LEVEL SHIFTER CIRCUIT
BUFFER CIRCUIT
PIXEL PORTION 604
SCANNING SIGNAL DRIVER CIRCUIT 605

Fig. 18

Fig. 19A

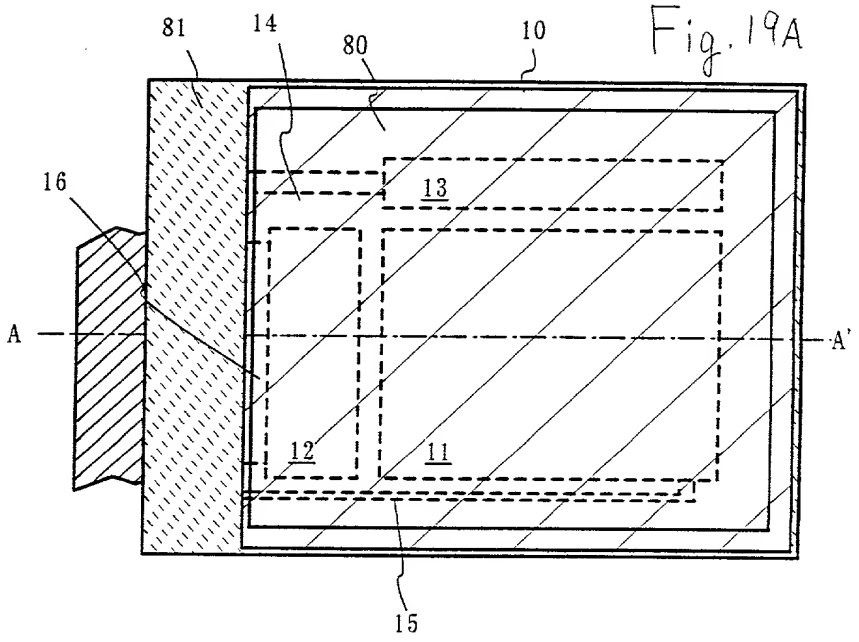


Fig. 19B

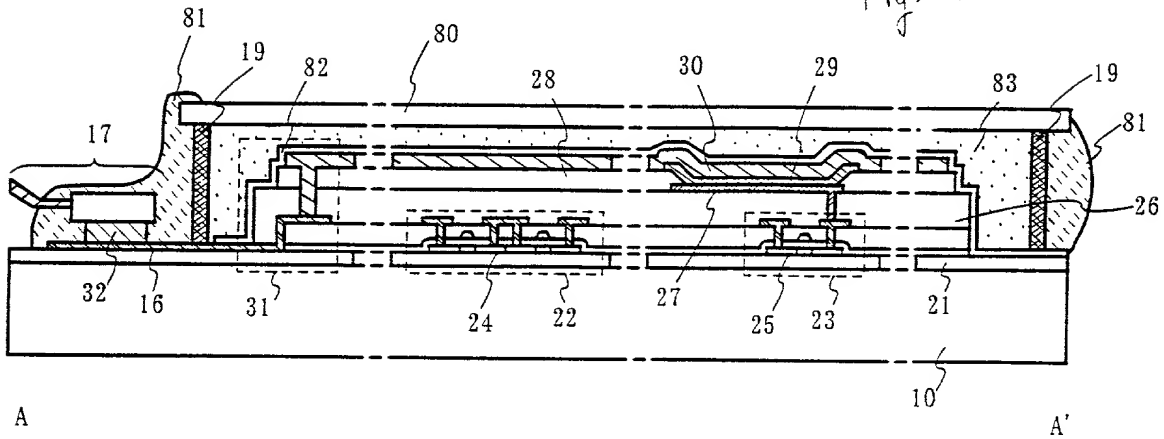


Fig. 20A

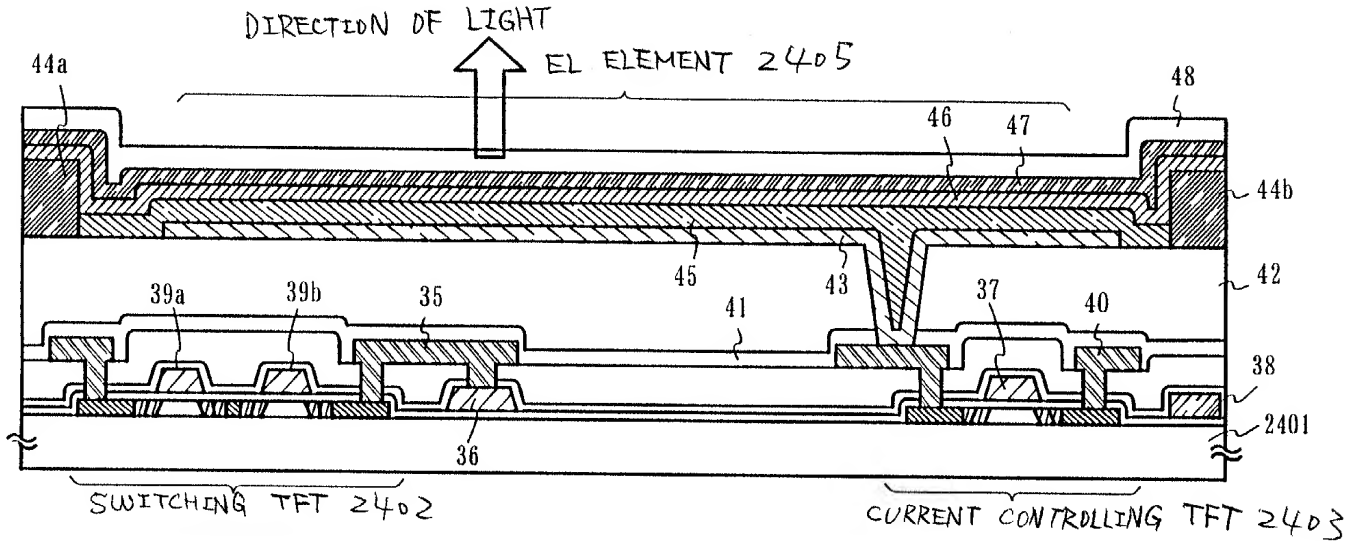
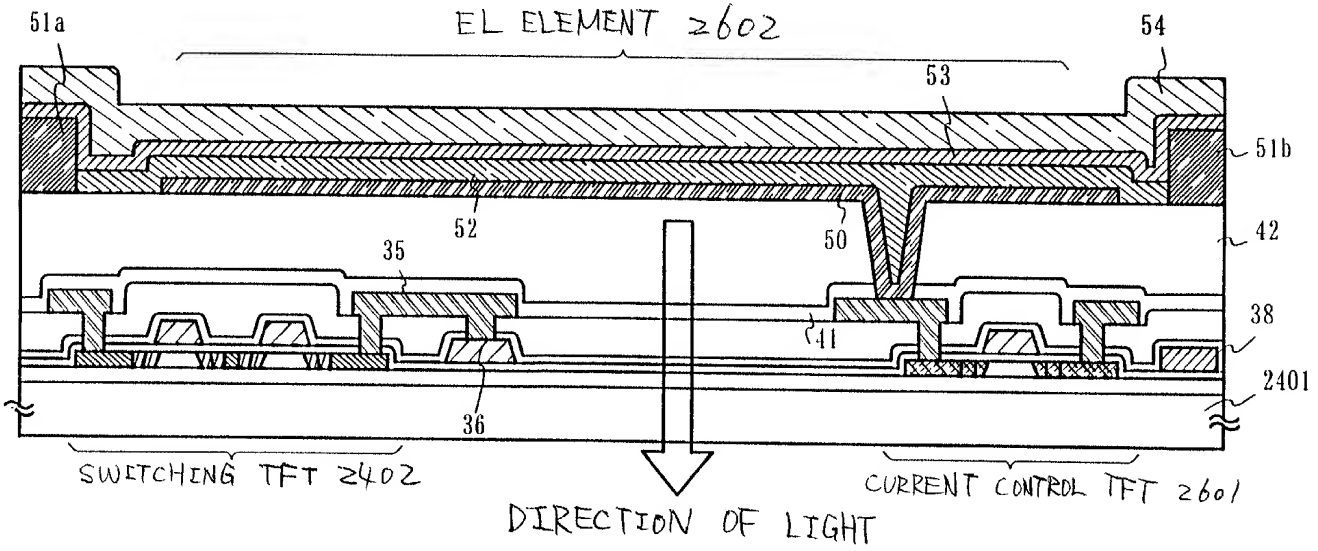


Fig. 20B



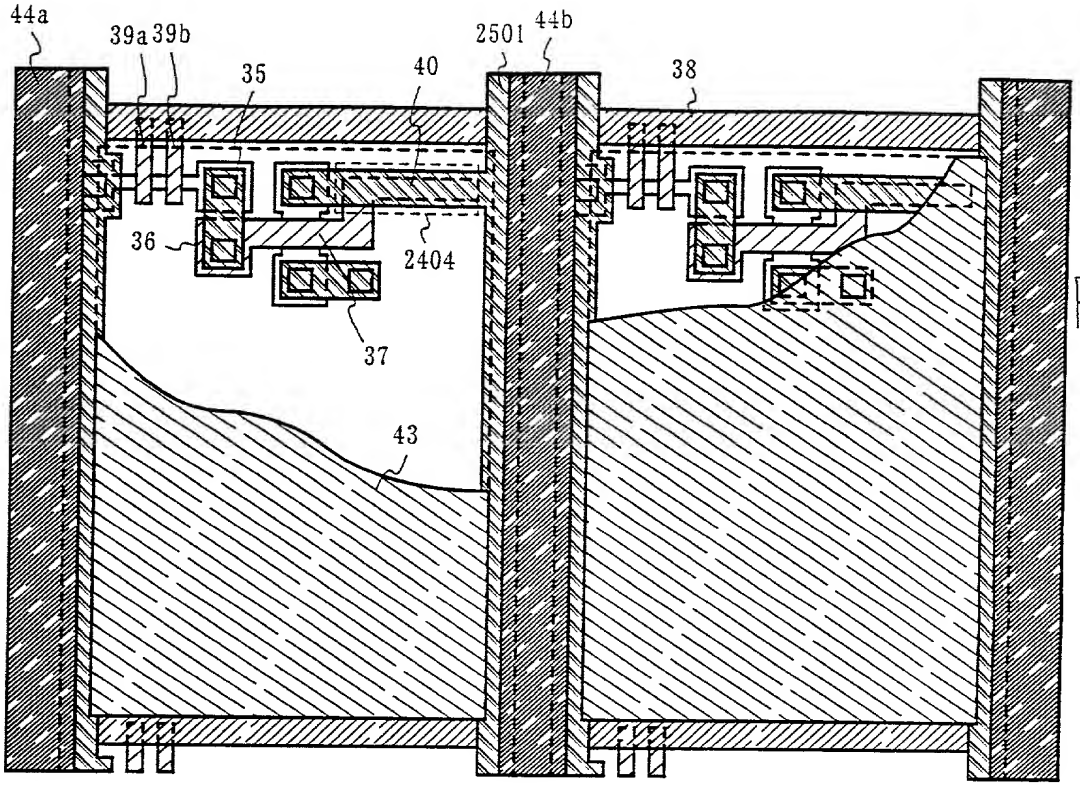
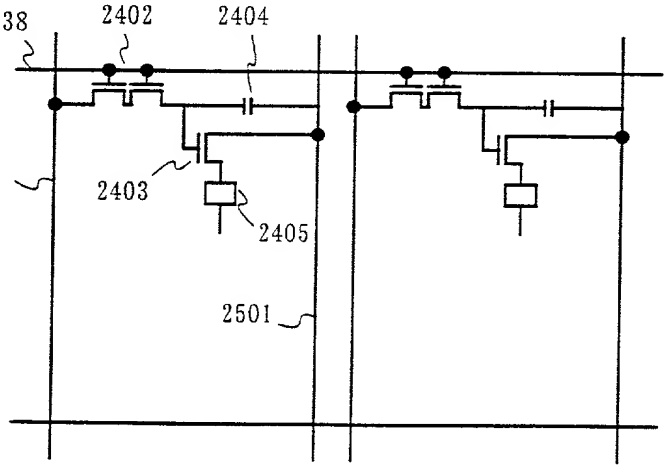


Fig. 21A



SOURCE WIRING

Fig. 21B

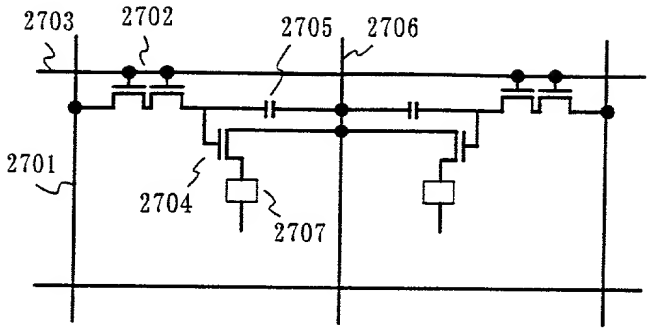


Fig. 22A

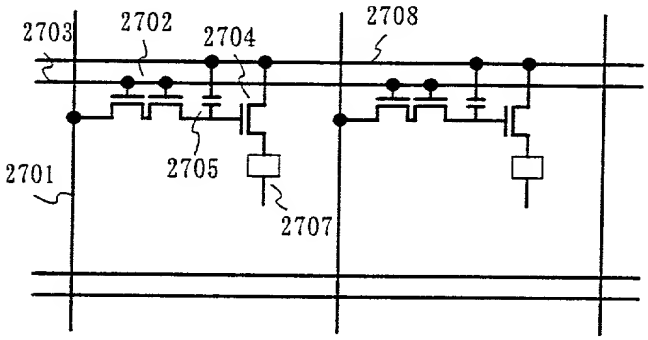


Fig. 22B

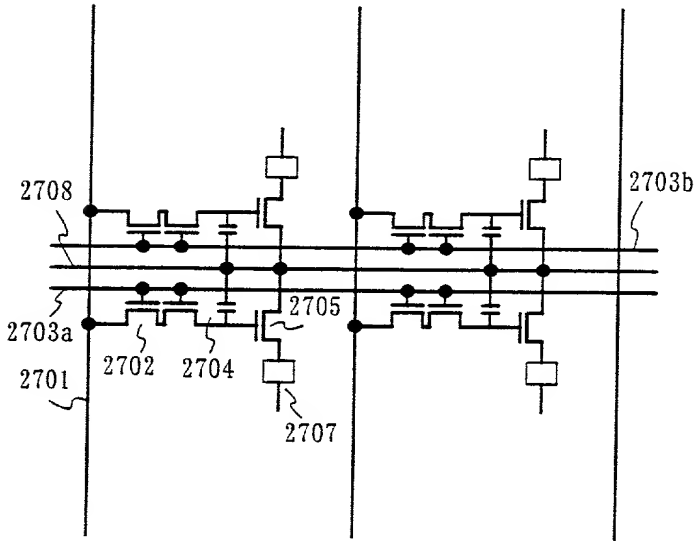


Fig. 22C

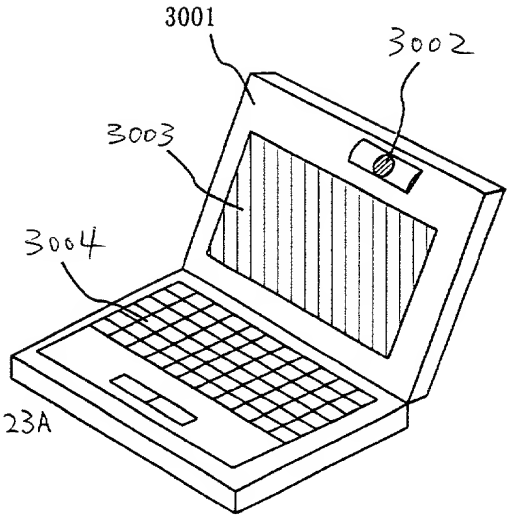


Fig. 23A

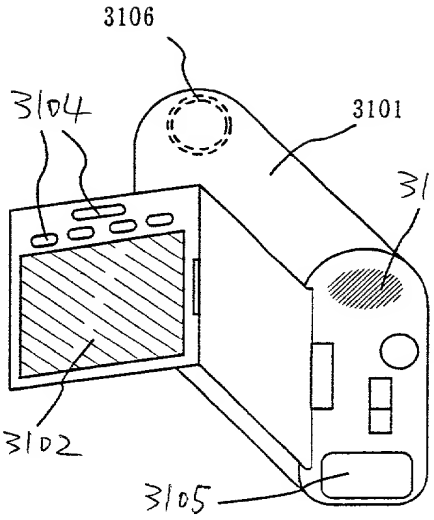


Fig. 23B

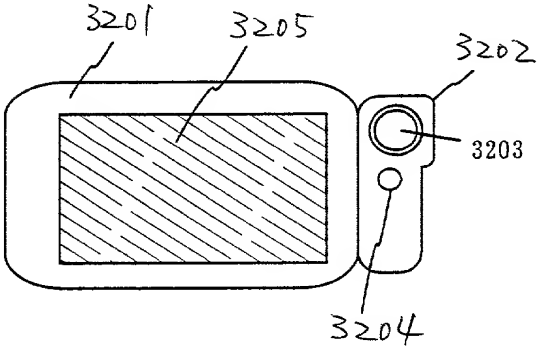


Fig. 23C

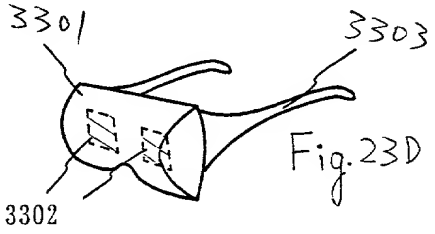


Fig. 23D

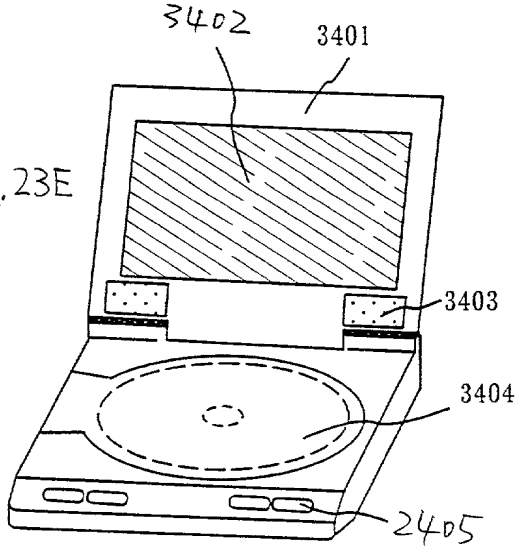


Fig. 23E

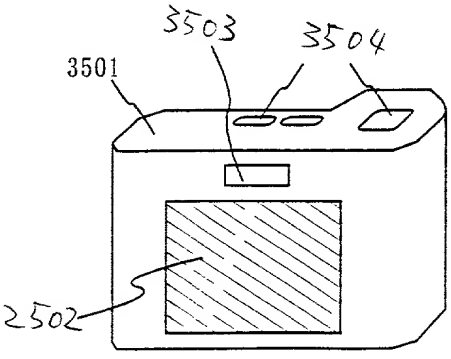
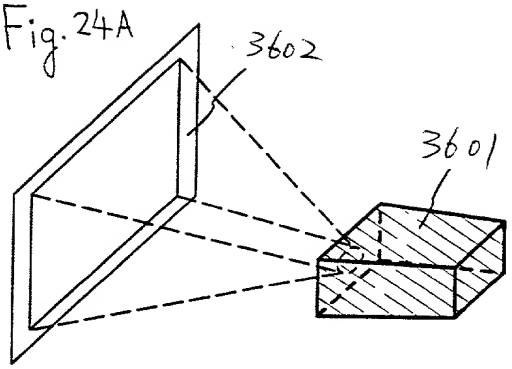


Fig. 23F

Fig. 24A



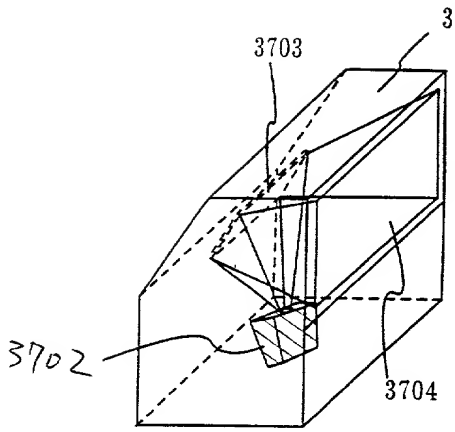


Fig. 24B

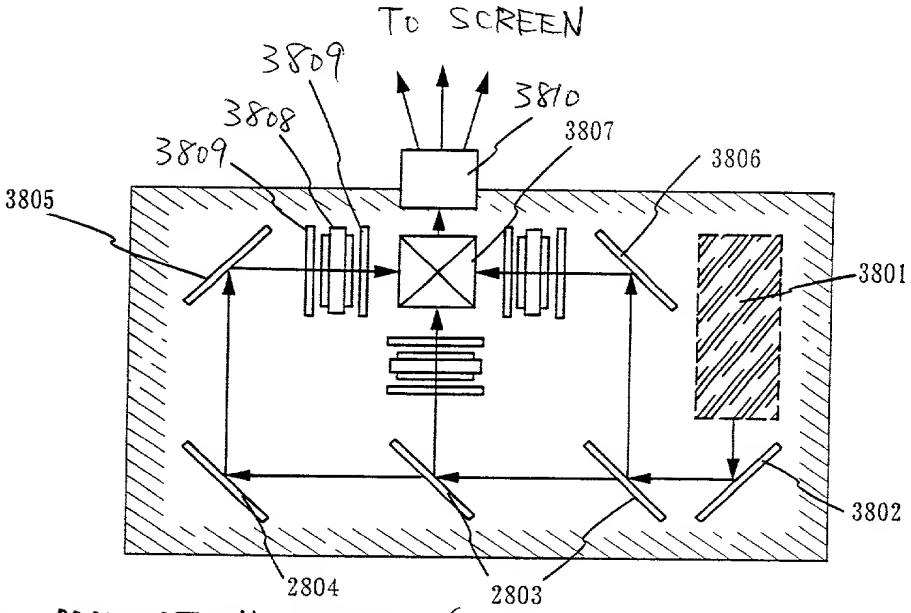


Fig. 24C PROJECTION DEVICE (THREE PLATE TYPE)

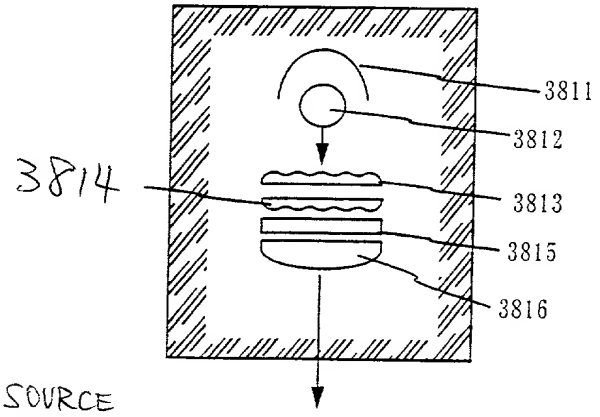


Fig. 24D LIGHT SOURCE OPTICAL SYSTEM

Fig. 25A

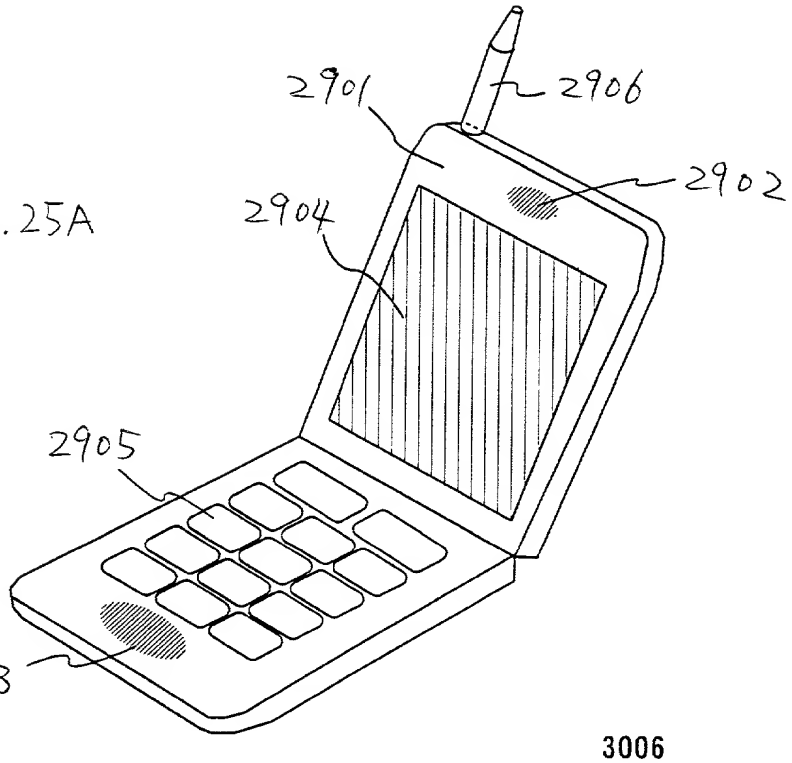


Fig. 25B

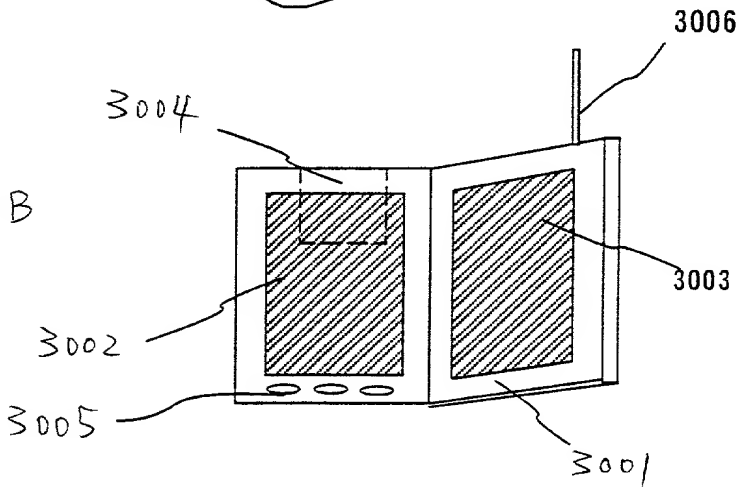


Fig. 25C

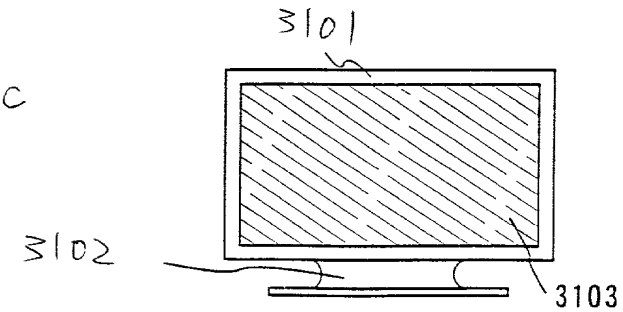


Fig. 26A

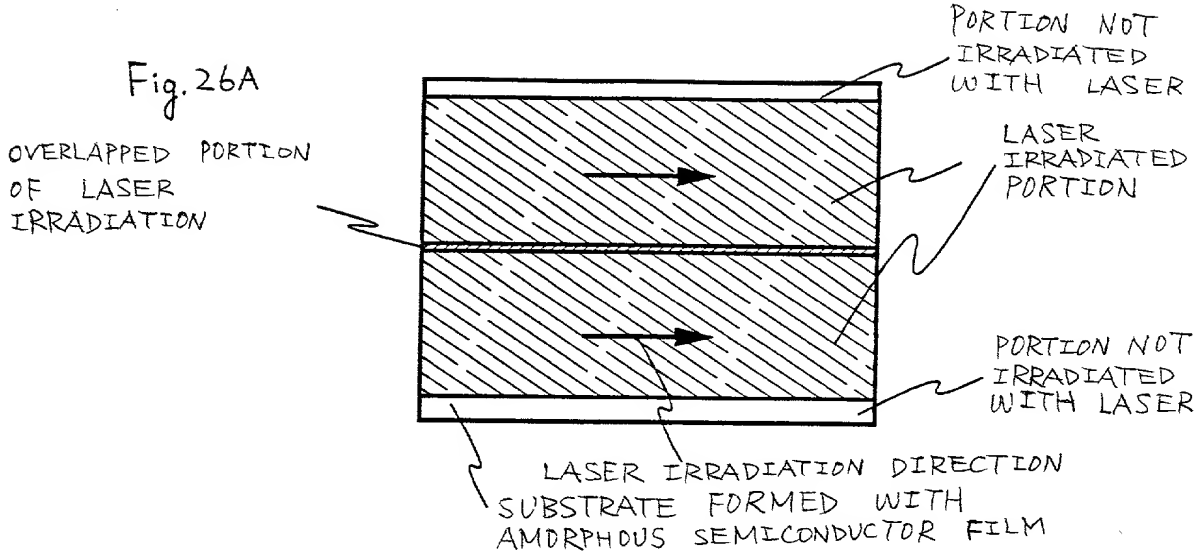


Fig. 26B

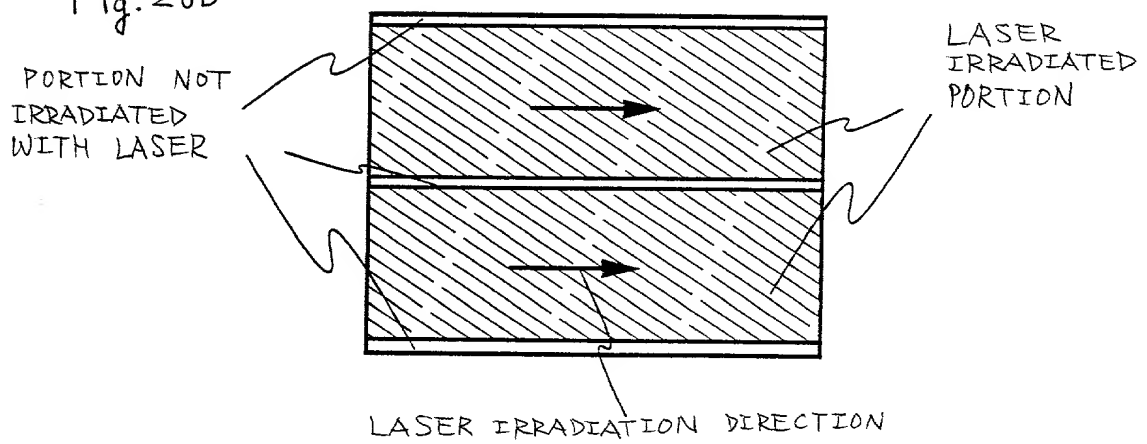


Fig. 26C